고속 **Row Cycle** 동작이 가능한 **VPM (Virtual Pipelined Memory)** 구조에 대한 연구

1998. 12. 28.

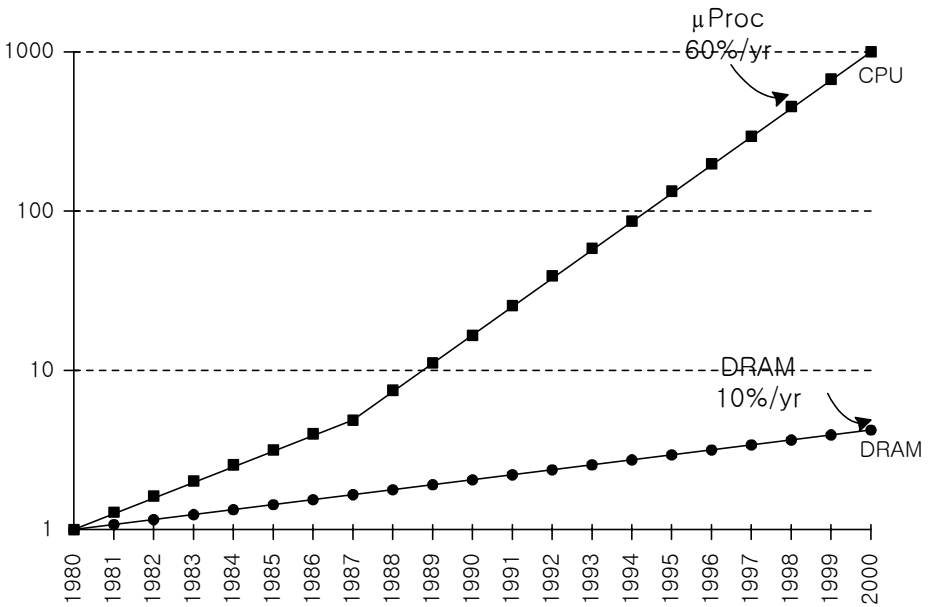
윤 치 원

발표 순서

- *연구의 필요성*
- 관련연구
- VCM (Virtual Channel Memory)
- POPeye : 메모리 시스템 성능 측정기
- POPeye를 이용한 VCM 분석
- VPM (Virtual Pipelined Memory)
- 결론 및 추후과제

연구의 필요성 (1)

- Memory와 Processor의 Performance Gap
  - 전체 시스템 성능을 제한



- 1980 : no cache(HW controlled buffer) in µprocessor
- 1980 : 64kb DRAM

연구의 필요성 (2)

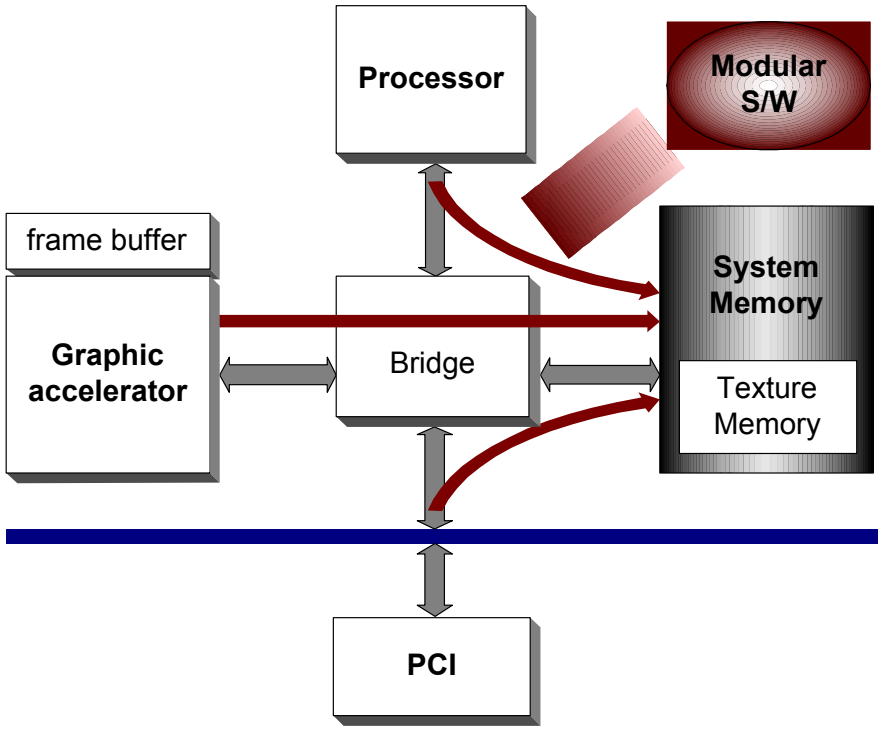
❑ Peak Bandwidth 향상을 위한 노력

$$Bandwidth = Bus\ \ Width \times I/O\ \ Frequency$$

- Wide Data Bus
- Column Path의 고속화
  - EDO, 3-stage Pipeline, Wave Pipeline
- Interface의 개선
  - D-RDRAM, SLDRAM
- ***Random 한 Row Access 에 대해 Effective Bandwidth 저하 !!***

연구의 필요성 (3)

- Today's Computer System
  - ⇨ ***Random Access Pattern on System Memory***



발표 순서

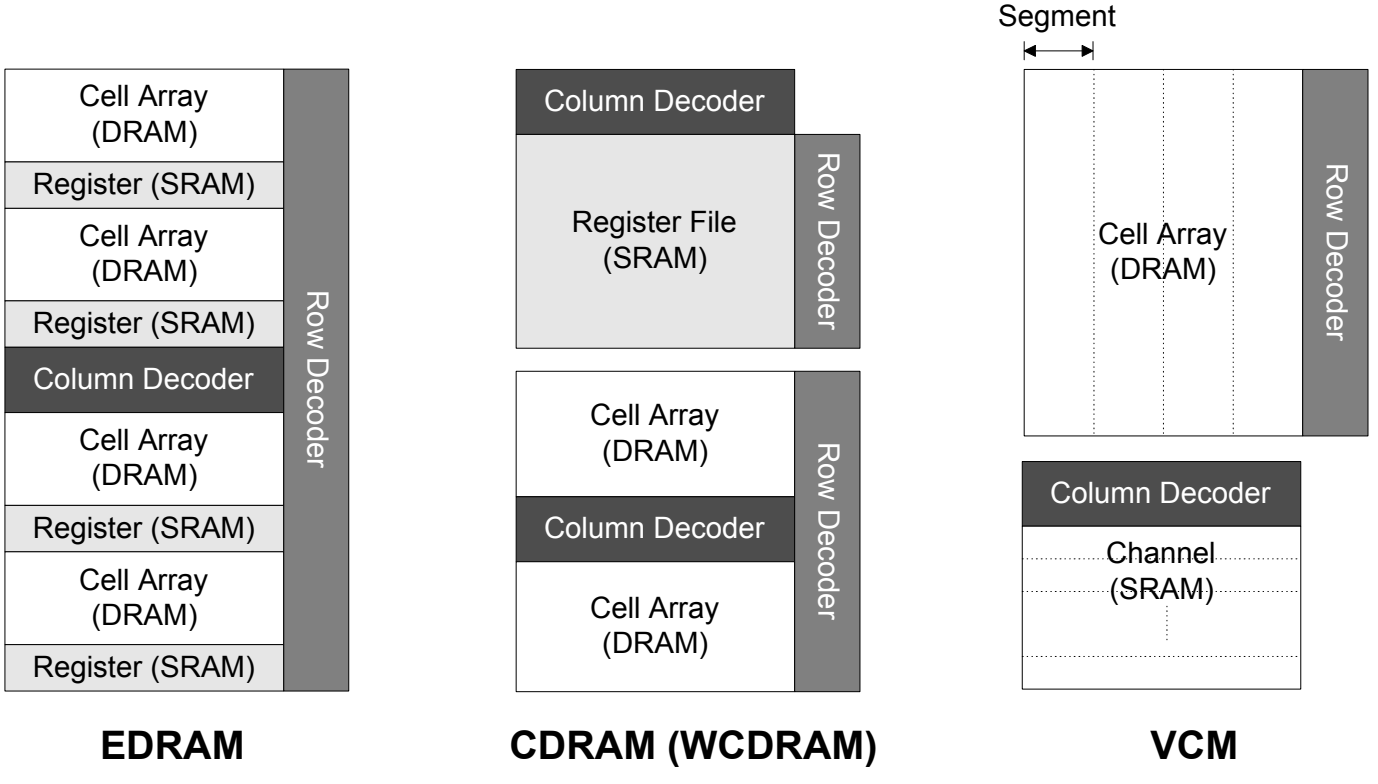
- 연구의 필요성
- *관련연구*
- VCM (Virtual Channel Memory)
- POPeye : 메모리 시스템 성능 측정기
- POPeye를 이용한 VCM 분석
- VPM (Virtual Pipelined Memory)
- 결론 및 추후과제

관련 연구(1)

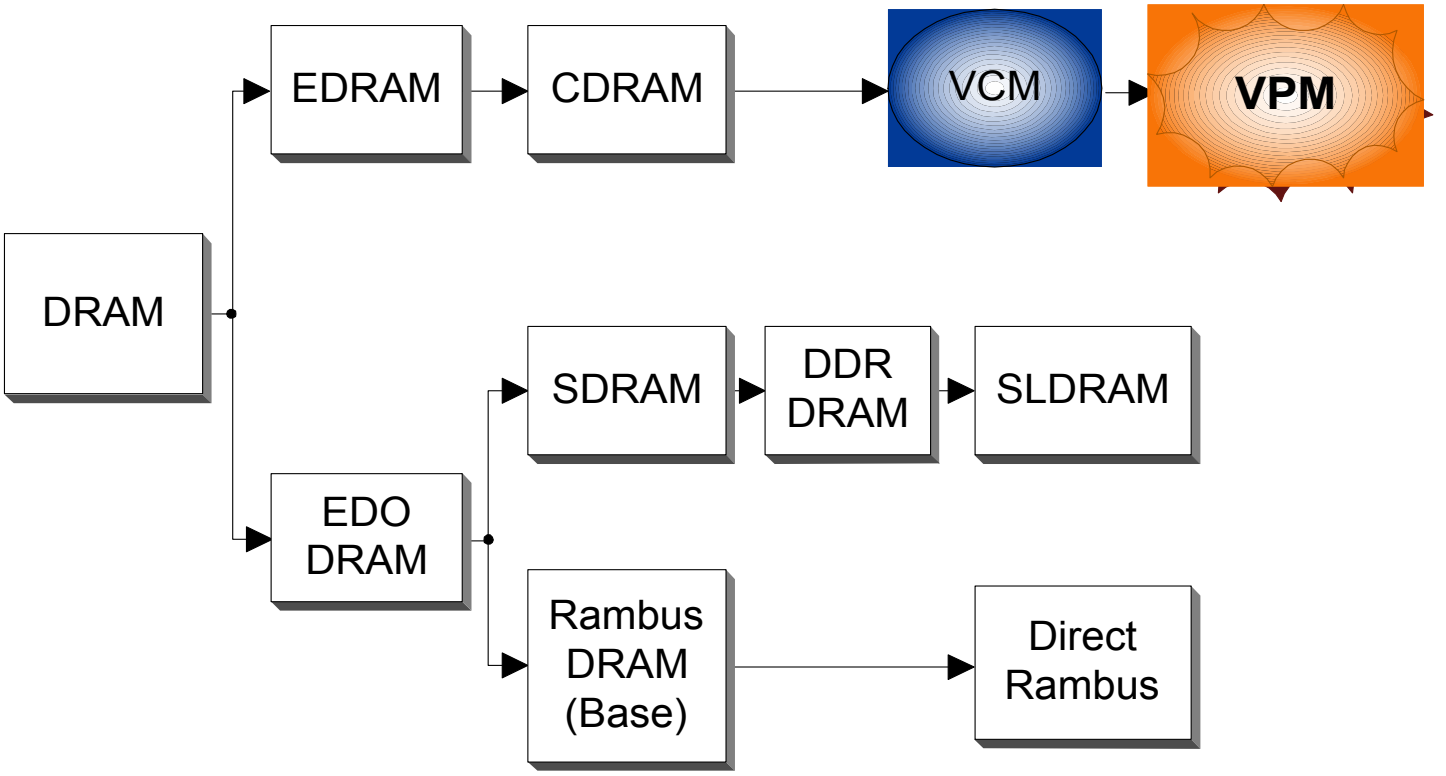
- Reduction of Random Row Cycle
  - Multi Bank Structure (1994, MoSys)
  - Temporal Storage Buffer (S. Wakayama, Fujitsu, SOVC'98)
  - Small Block Access
    - FCRAM (Y. Sato, Fujitsu, SOVC'98)
  - Integration of SRAM
    - Hierarchical Structure
    - EDRAM(1992, EDRAM), CDRAM(1992, Mitsubishi), W-CDRAM(Duke Univ., 1997), VCM(1998, NEC)

관련 연구(2)

❑ Comparison of SRAM Integrated Structure



VPM


DRAM
EDRAM
CDRAM
VCM
VPM
SDRAM
DDR DRAM
SLDRAM
EDO DRAM
Rambus DRAM (Base)
Direct Rambus

발표 순서

- 연구의 필요성
- 관련연구
- *VCM (Virtual Channel Memory)*
- POPeye : 메모리 시스템 성능 측정기
- POPeye를 이용한 VCM 분석
- VPM (Virtual Pipelined Memory)
- 결론 및 추후과제

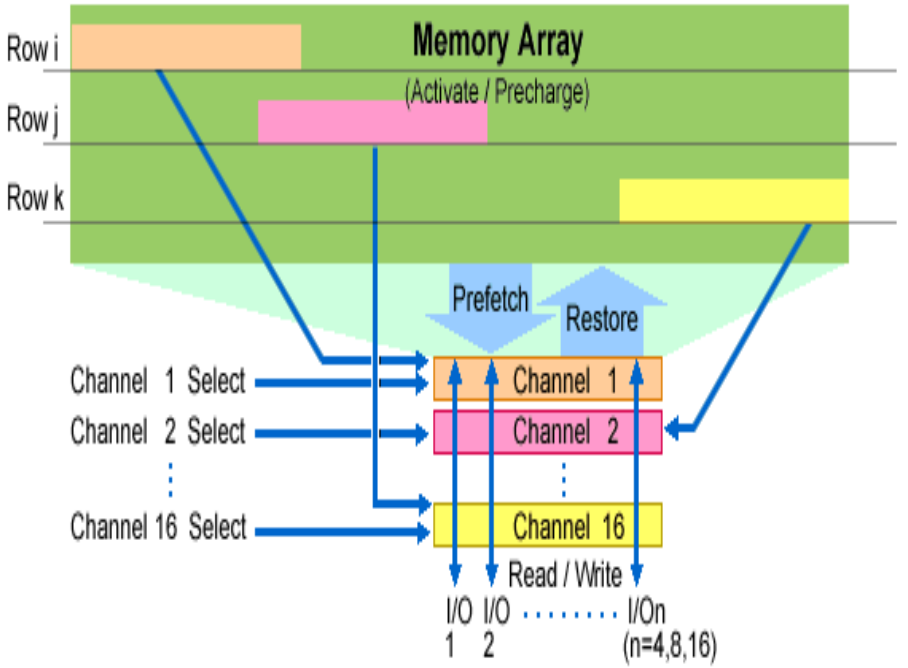
VCM (Virtual Channel Memory)

- 개요
  - Integration of SRAM Buffer in DRAM
    - Channel
  - Cell Core 구조의 변형
    - Backward Compatibility
  - External Controller에 의한 Data Transfer Control
    - 면적 증가 억제
    - Flexibility

VCM (Virtual Channel Memory)

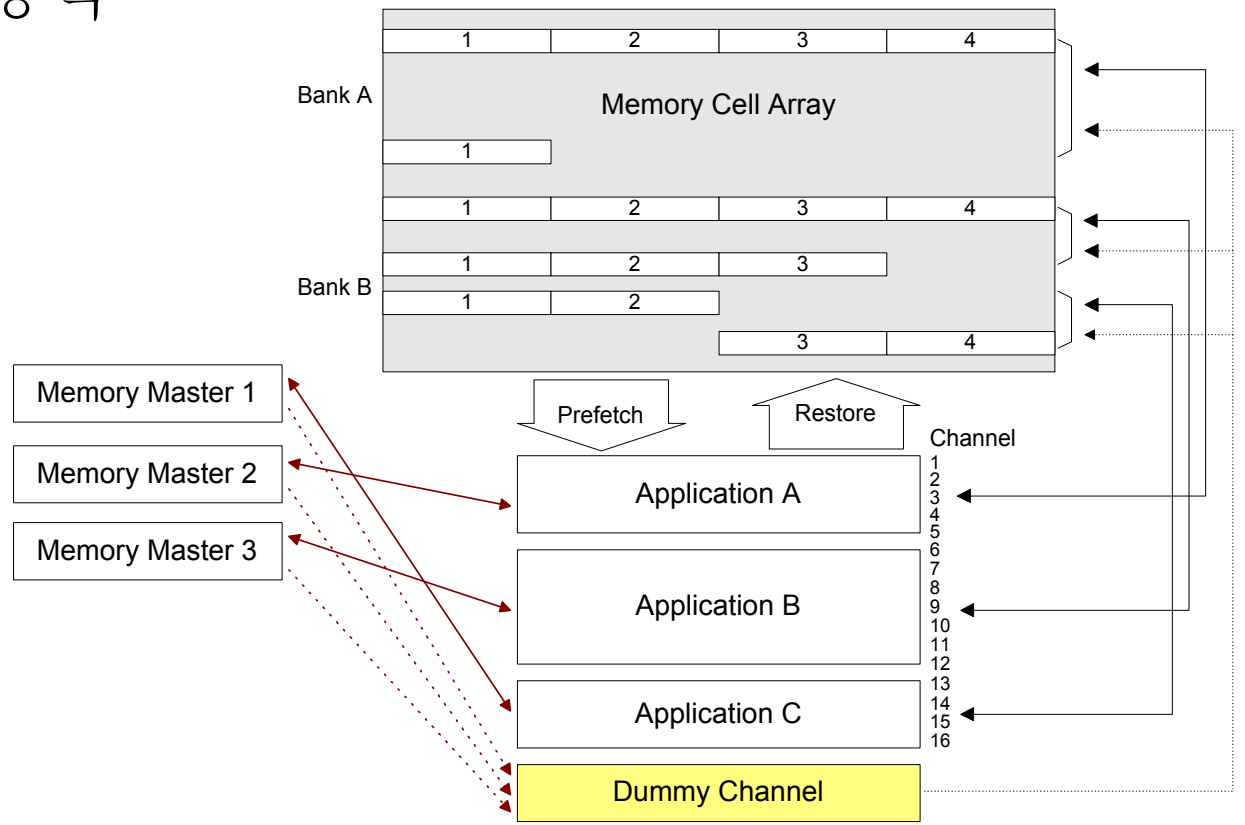
❑ 구조 및 동작 원리

- Channel
  - Fully associative
  - 16 + 1 Channel(Dummy)
- Segment (1Kbit)
- SRAM Access
  - Foreground Operation
  - Channel Read, Write
- Cell Core Access
  - Background Operation
  - Prefetch, Restore



VCM (Virtual Channel Memory)

❑ VCM의 동작



발표 순서

- 연구의 필요성
- 관련연구
- VCM (Virtual Channel Memory)
- *POPeye : 메모리 시스템 성능 측정기*
- POPeye를 이용한 VCM 분석
- VPM (Virtual Pipelined Memory)
- 결론 및 추후과제

메모리 시스템 성능 측정기

❑ 필요성

– 현재의 Computer System
  - 다양한 Access Pattern의 Application이 사용
  - 복잡한 Hardware Platform
  - H/W와 S/W가 서로 연관되어 유기적으로 동작

⇨ ***System*** *수준의 종합적 상황이 고려된 성능분석 필요 !!*

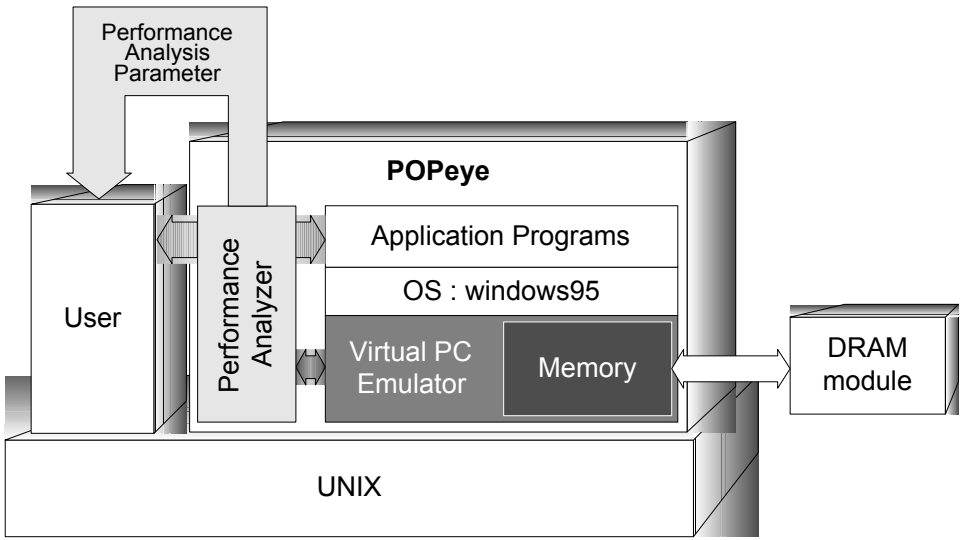
❑ 성능 측정기의 활용

– Comparison of Performance

– ***TOP-down*** *방식의* ***Memory Design*** *방식 제공*

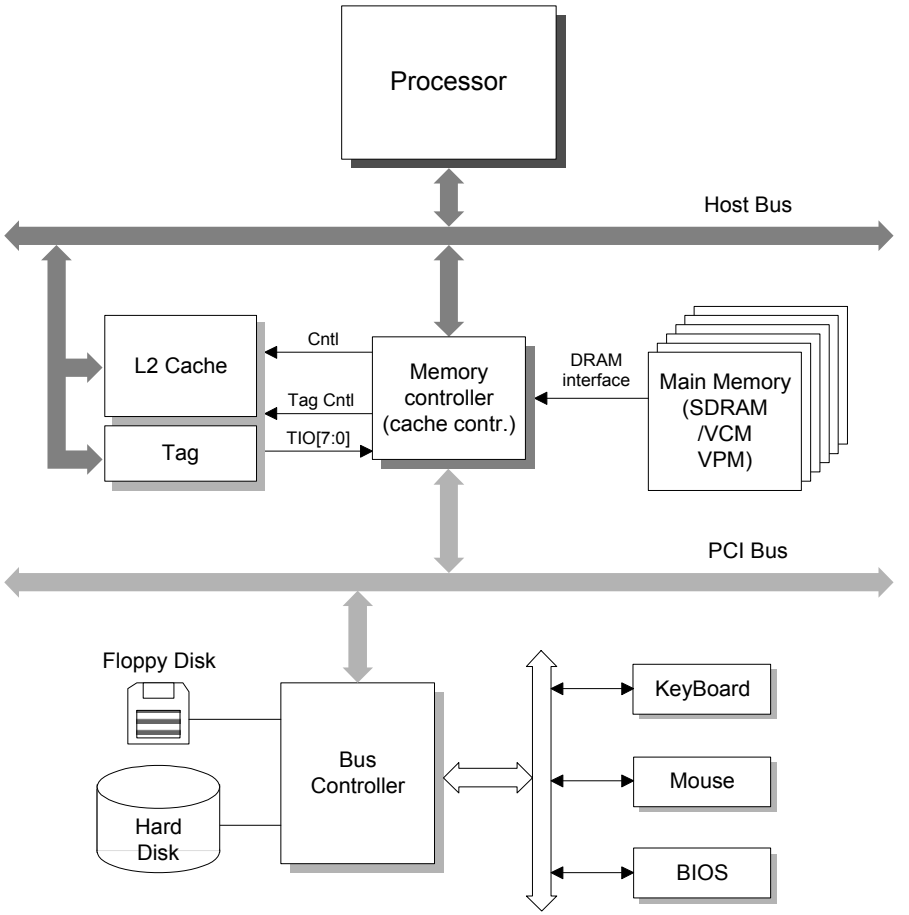
POPeye (1)

- POPeye
  - System의 종합적인 행동양식을 고려한 Memory System 성능 측정기
  - H/W Platform + System Software + Application



POPeye (2)

- Target System
  - PC system
    - x86 계열 CPU
    - Internal L1 Cache
    - External L2 Cache
    - External Devices
    - Memory Controller
    - System Memory



발표 순서

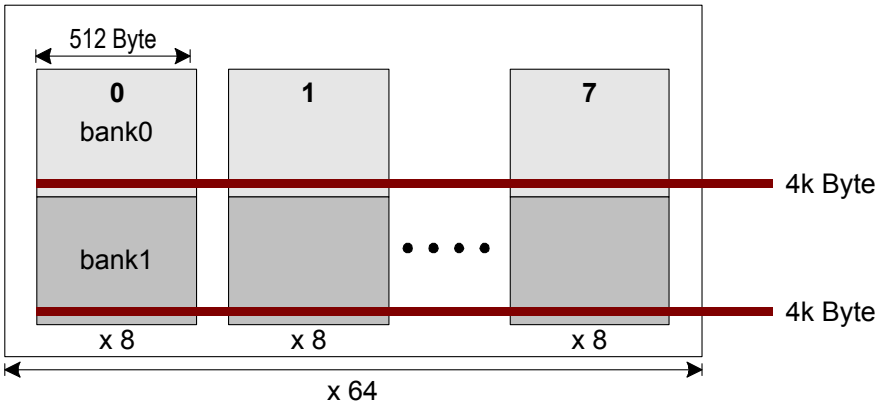
- 연구의 필요성
- 관련연구
- VCM (Virtual Channel Memory)
- POPeye : 메모리 시스템 성능 측정기
- *POPeye를 이용한 VCM 분석*
- VPM (Virtual Pipelined Memory)
- 결론 및 추후과제

POPeye를 이용한 VCM 성능 분석

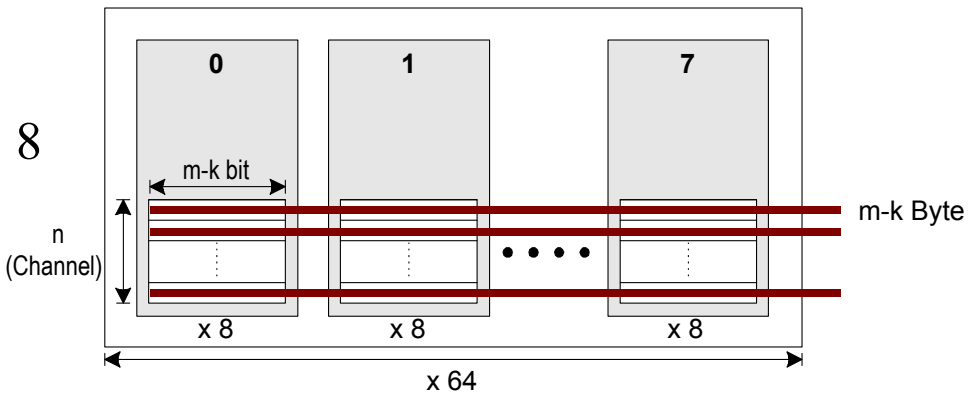
❑ Memory Modeling

- SDRAM Module
  - 64MB : (64MBit × 8) × 8
  - Chip Organization
    - (8096× 512) × 2
    - ×8 I/O
- VC-SDRAM Module
  - 64MB : (64MBit × 8) × 8
  - Chip Organization
    - (8096× 512) × 2
    - ×8 I/O

SDRAM : Open page = 4KB x 2 = 8KB



VC-SDRAM : Open page = (n x mk bit) x 8 = nxm KB

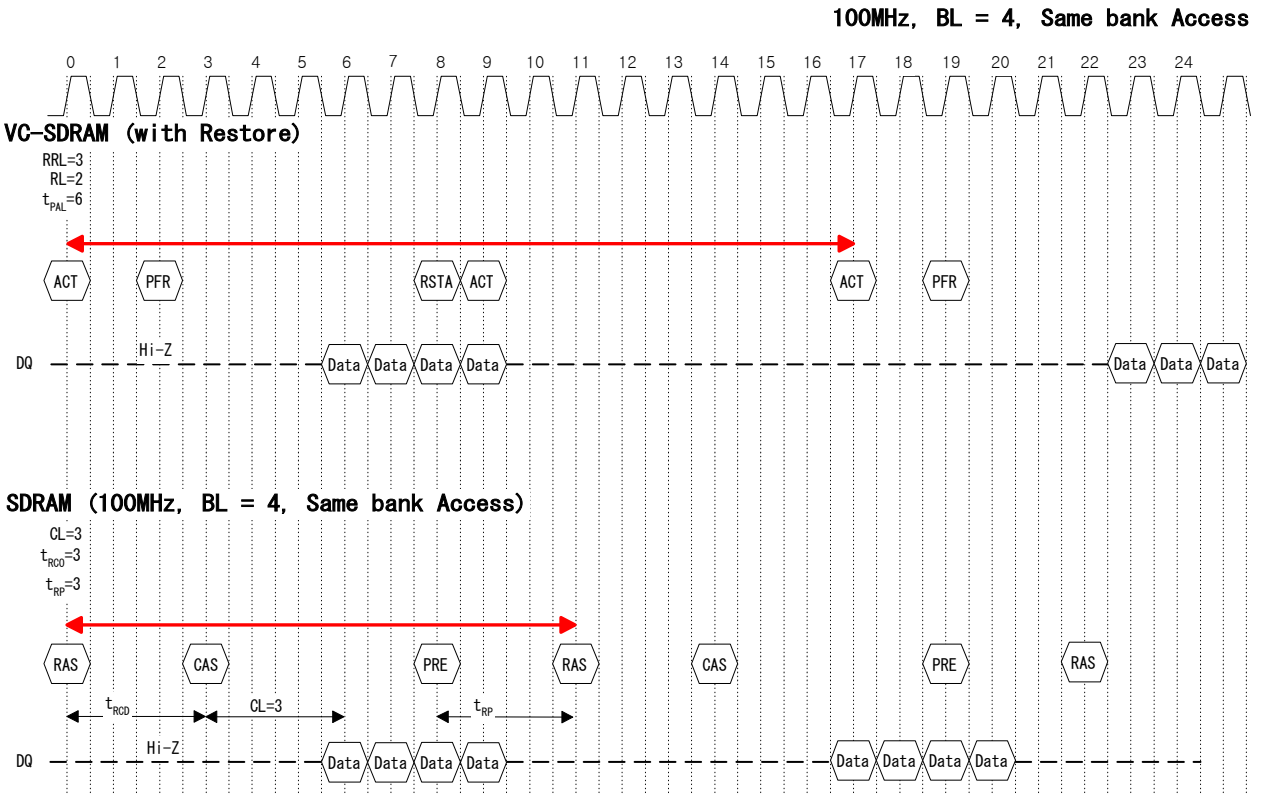


POPeye Simulation

- Issues on Channel
  - Number Of Channels
  - Channel Width
    - 1 Row Prefetch Vs. 1/4 Row Prefetch
  - Dummy Channel Access
    - Write Allocation Vs. No-Write-Allocation
- Latency Comparison
  - Channel(Page) Hit
    - Same Latency
  - Channel(Page) Miss
    - Read Miss : Same or Long(Restore)
    - Write Miss : Short (Dummy Hit) or Long(Dummy Miss)

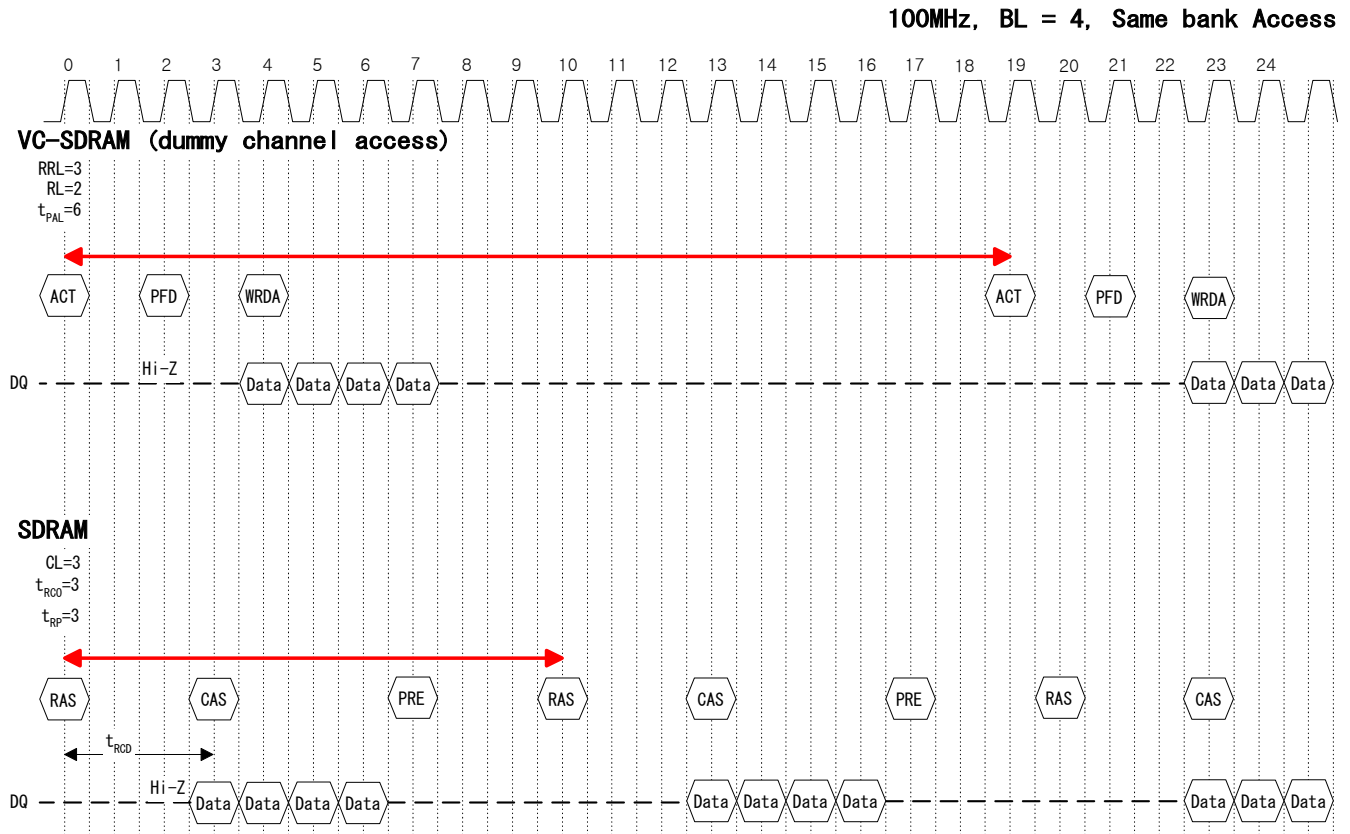
POPeye Simulation

❑ Latency Comparison (Read Miss Cycle)



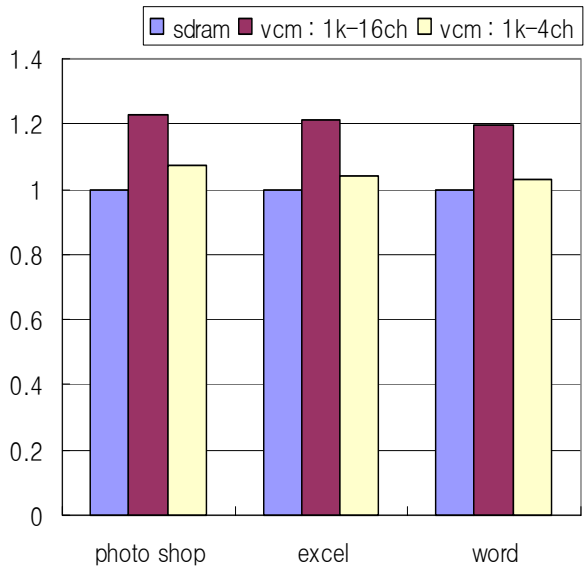
POPeye Simulation

❑ Latency Comparison(Write Miss Cycle)

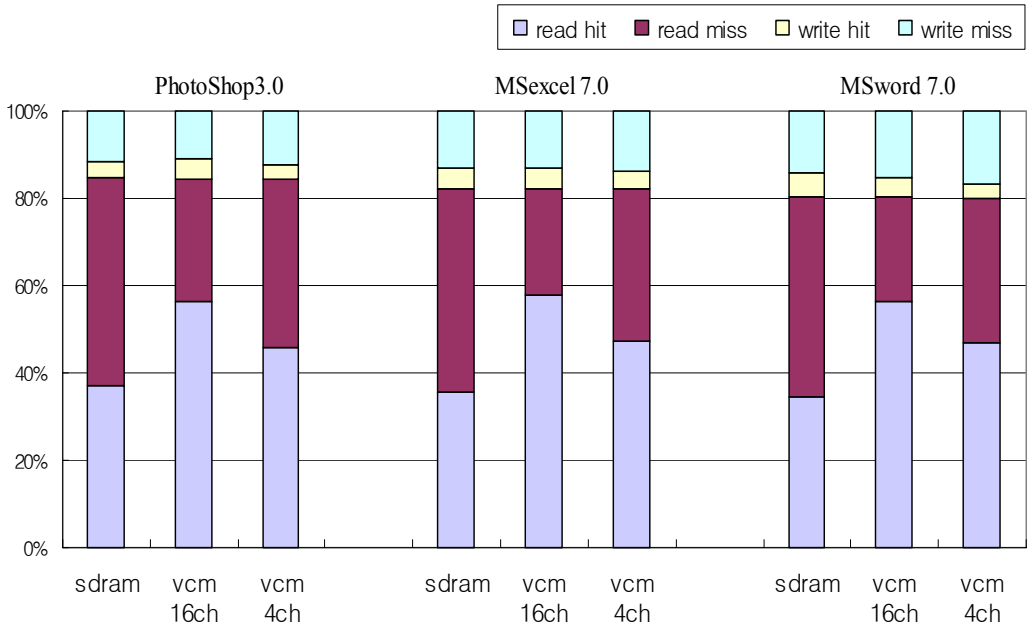


Simulation Result

❑ Channel 개수에 따른 특성 변화



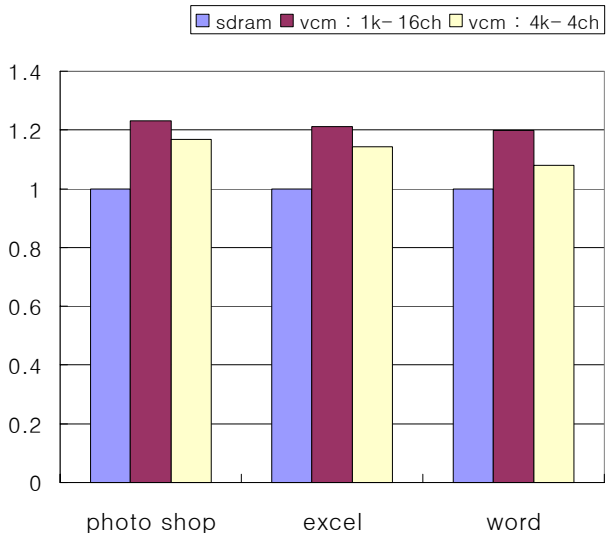
Performance



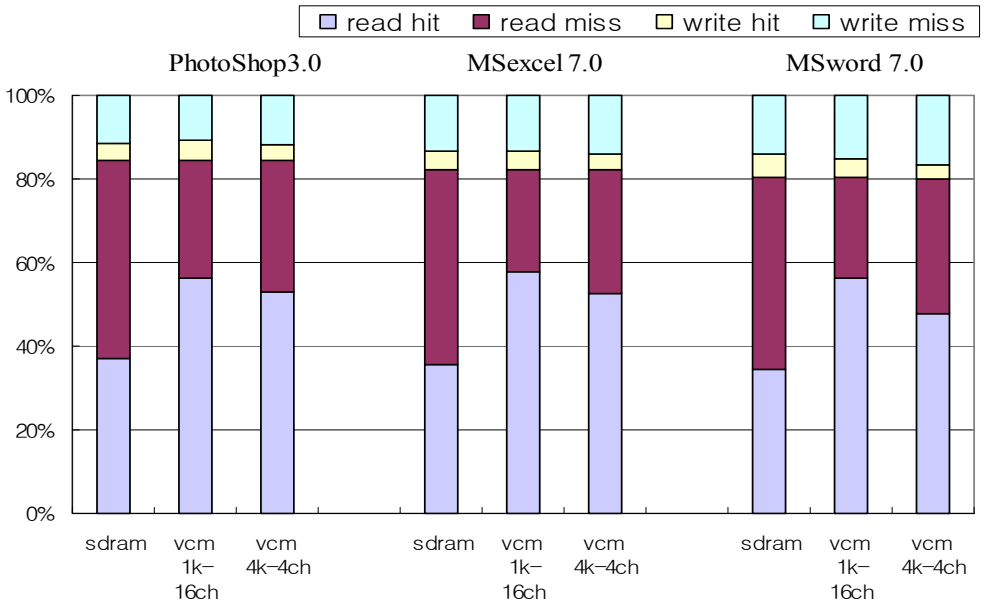
Access Pattern

Simulation Result

❑ Channel 길이에 따른 특성 변화



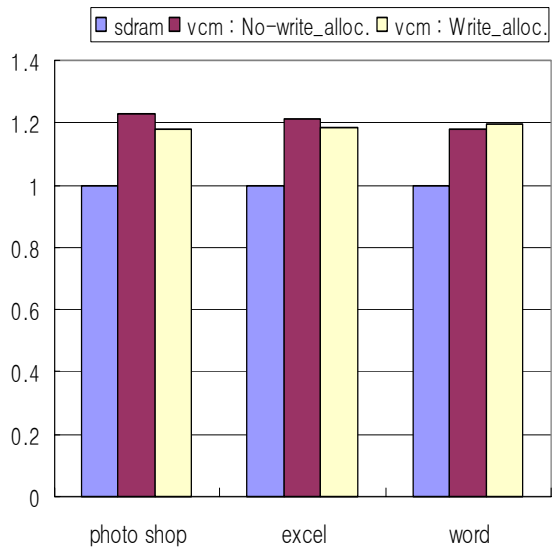
Performance



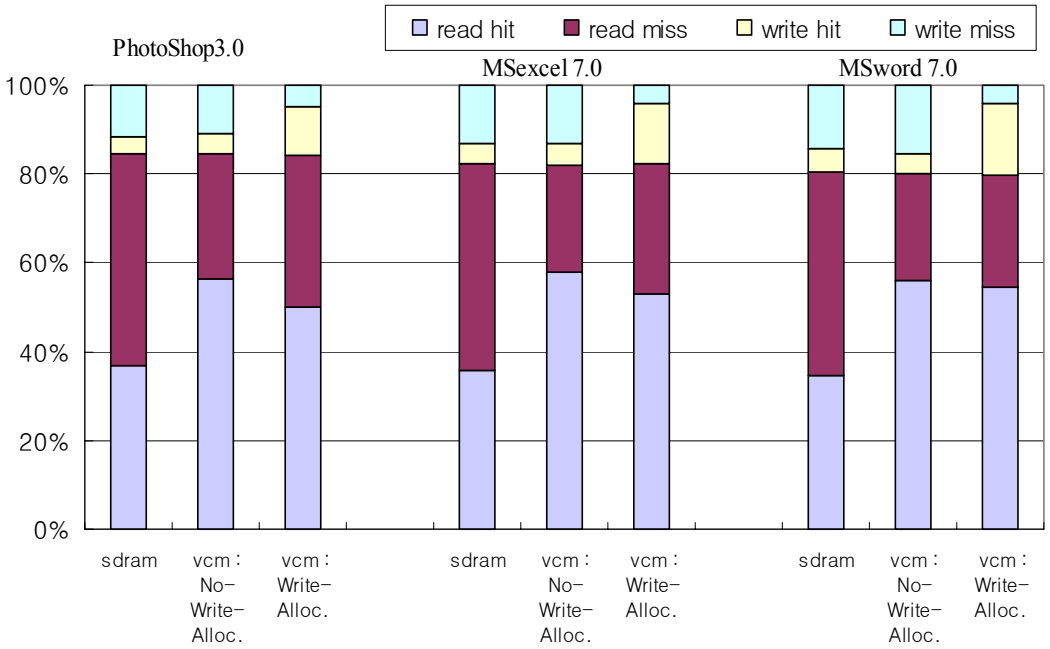
Access Pattern

Simulation Result

❑ Dummy Channel Access 방식에 따른 변화



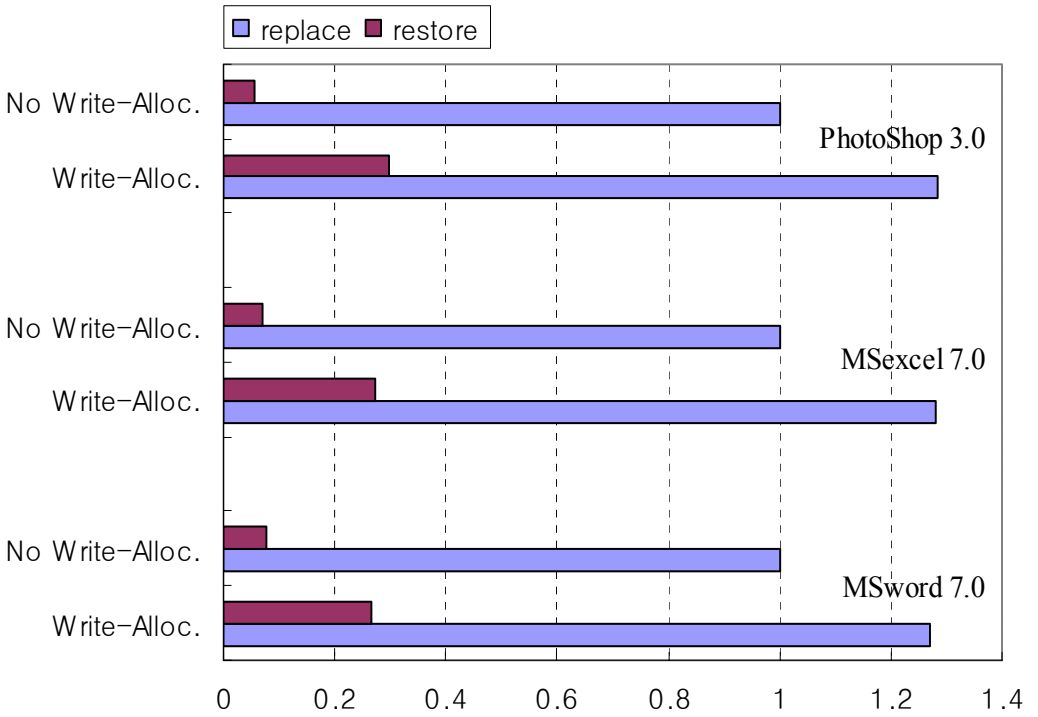
Performance



Access Pattern

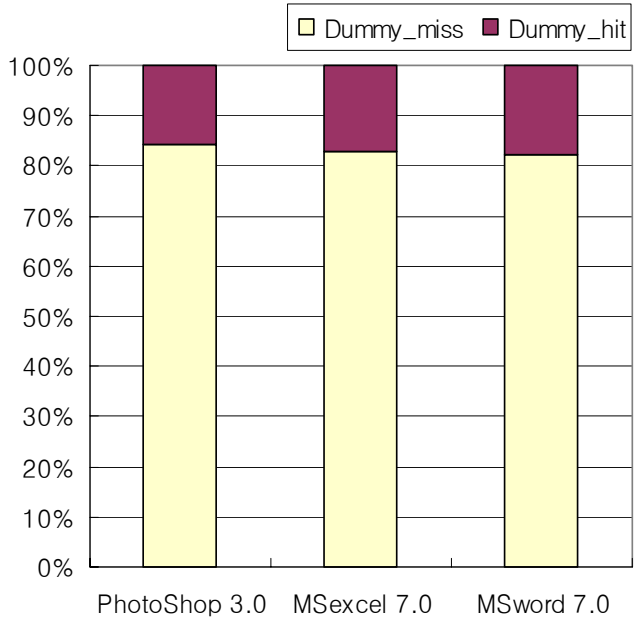
Simulation Result

❑ Channel Replace & Restore

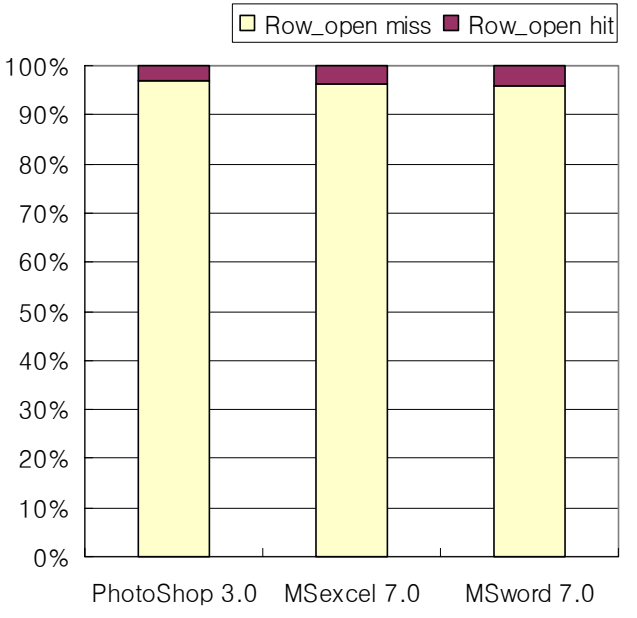


Simulation Result

❑ Channel Access Pattern(for 16 Channels)



Dummy Channel Hit Ratio



Opened Row Hit Ratio

결과 분석

❑ 결과 분석

– Performance Improvement

- With Integrating Only 4 Channels
- With 1/4 Row Prefetching Scheme
- With “No Write Allocation” Method

– Characteristics of Background Operations

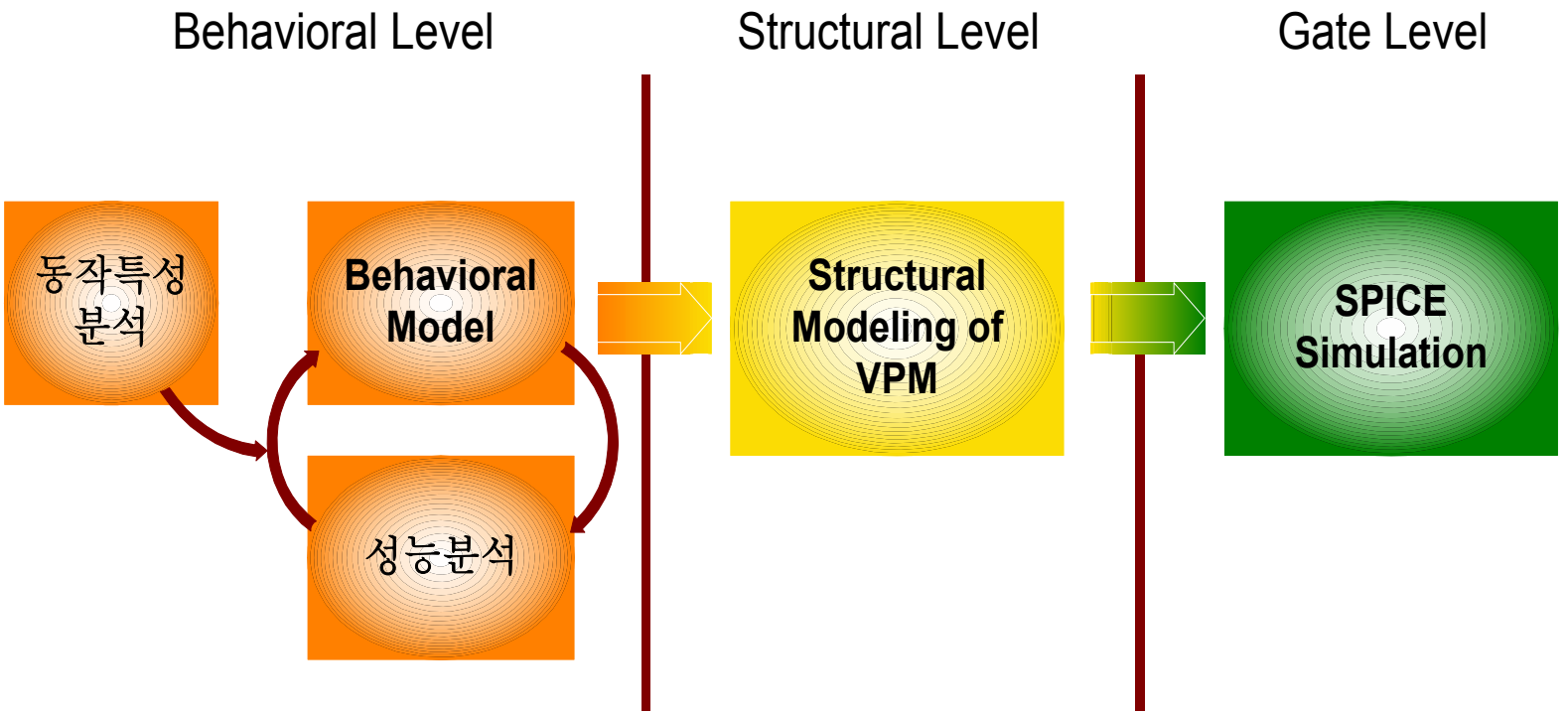
- Poor Utilization of Previously Activated Row
- Poor Hit Ratio for Dummy Channel in the Case of Successive Write Miss Cycle

– Performance Limited by Background Operations !!

발표 순서

- 연구의 필요성
- 관련연구
- VCM (Virtual Channel Memory)
- POPeye : 메모리 시스템 성능 측정기
- POPeye를 이용한 VCM 분석
- *VPM (Virtual Pipelined Memory)*
- 결론 및 추후과제

VPM (Virtual Pipelined Memory)



VPM Design (Behavioral Level)

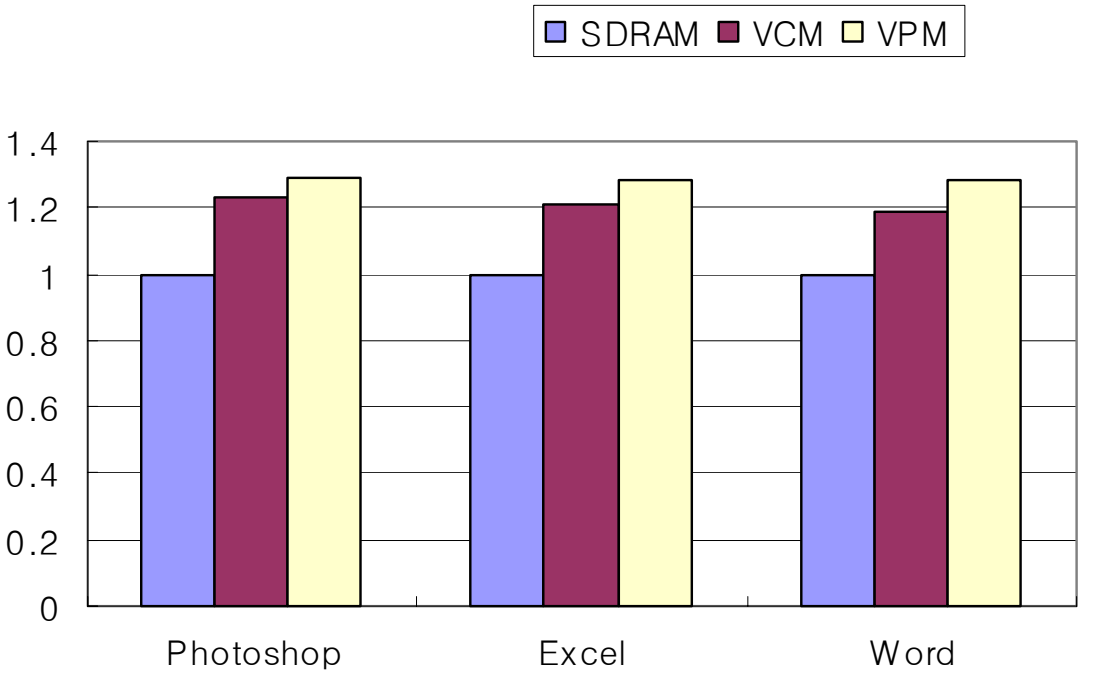
- From VCM Analysis Results,
  - Channel Structure is Effective
    - 1/4 Prefetching Scheme
    - "No Write Allocation"

- "No Write Allocation"
    - Long Write Miss Cycle
      - Read Modified Write for Dummy
        - » Prefetch to Dummy, Restore Dummy Data to Cell Core
      - Poor Dummy Channel Hit for Successive Write Miss Cycle

  ⇨ ***Use "Write Through"***

성능 분석 : VPM

- Performance Analysis
  - No Write Allocation with “Write Through”
  - 1/4 Prefetching, 16 channels



VPM Design (Behavioral Level)

❑ 1 Physical Row Activation

- 1 Physical Row Activation for Prefetching One Segment
- Poor Utilization of Previously Activated Row

⇨ ***"Partial Activation" 사용 !!***

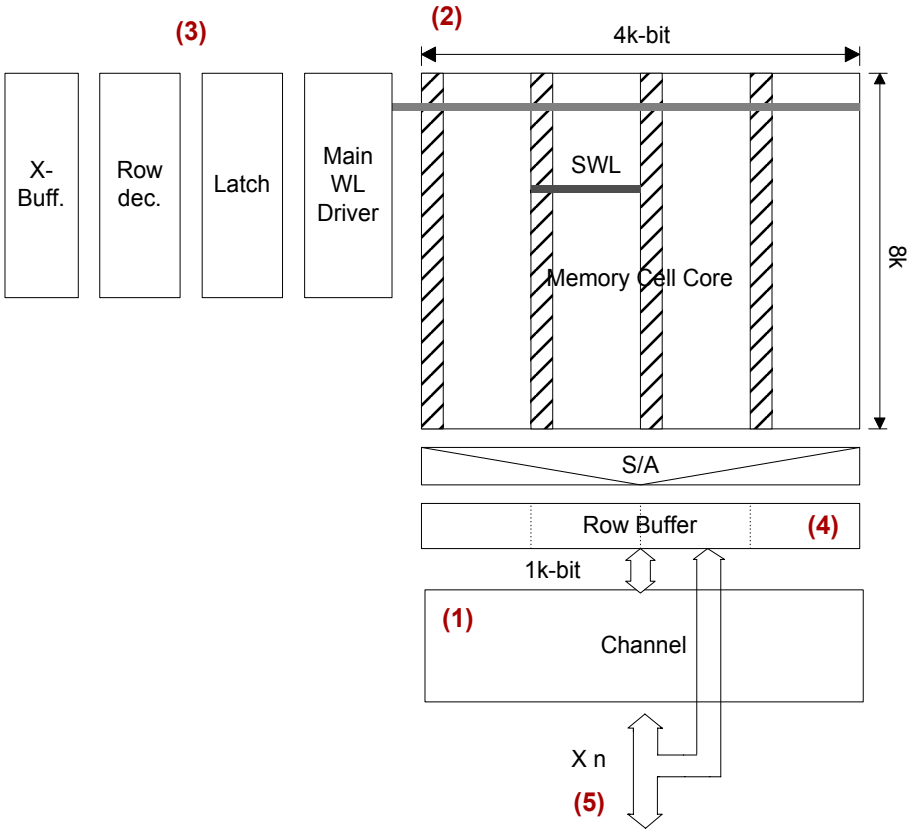
❑ Performance is Limited by Background Op.

- Fast Row Cycle을 위한 새로운 Scheme이 필요

⇨ ***Row Path Pipelining !!***

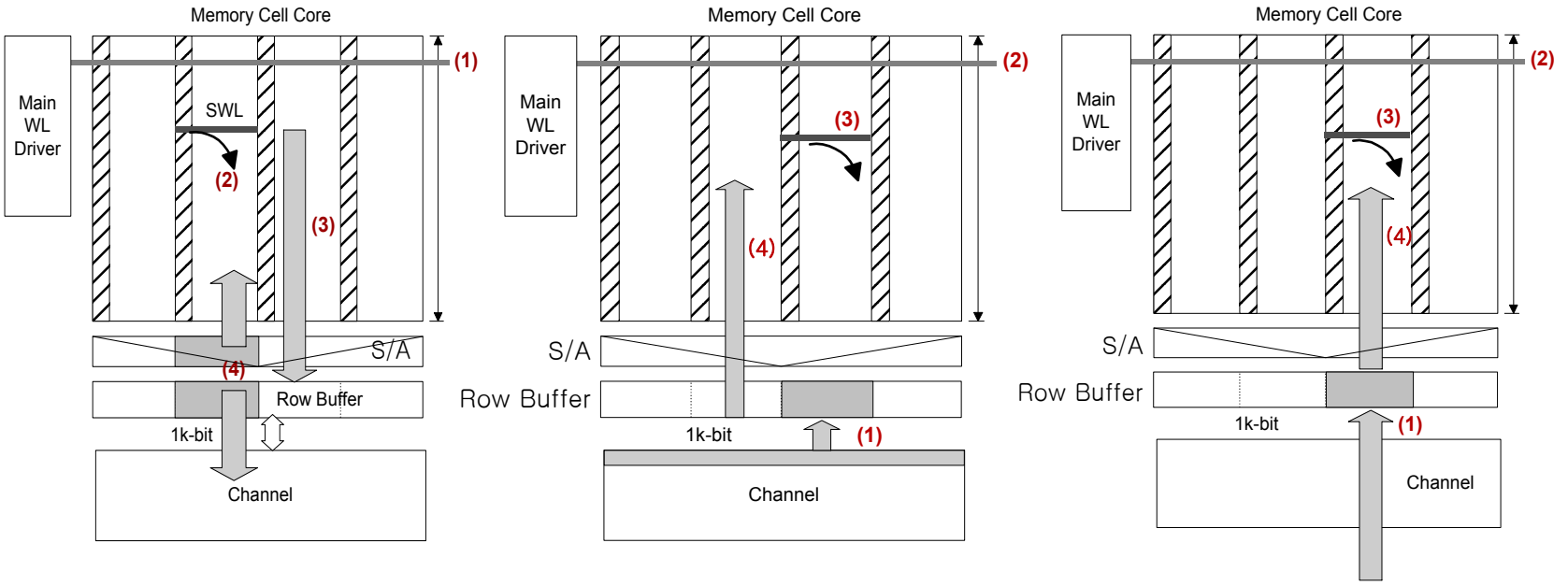
VPM Design (Structural Level)

- 기본 구조
  - (1) Channel
  - (2) Sub-WordLine 구조
    - Partial Activation
  - (3) Row Decoder Latch
  - (4) Row Data Buffer
  - (5) Direct Path to Row Buffer



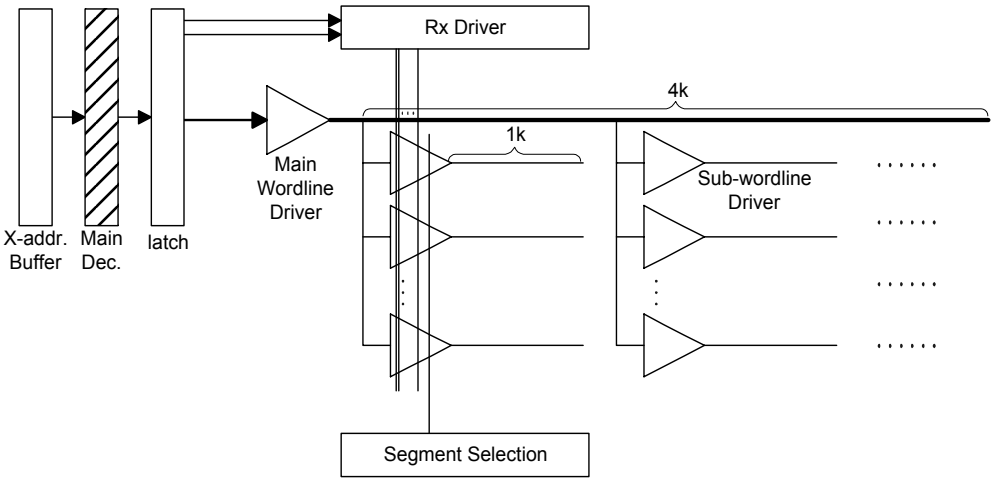
VPM Design (Structural Level)

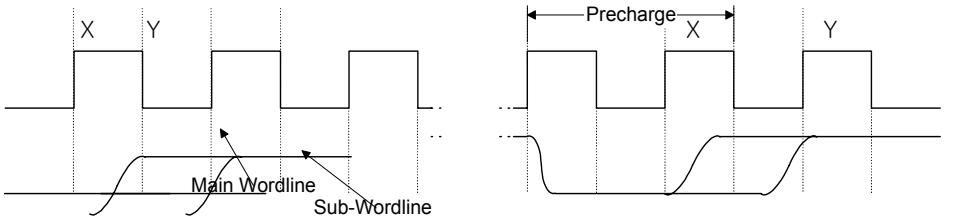
❑ Background Operations



VPM Design (Structural Level)

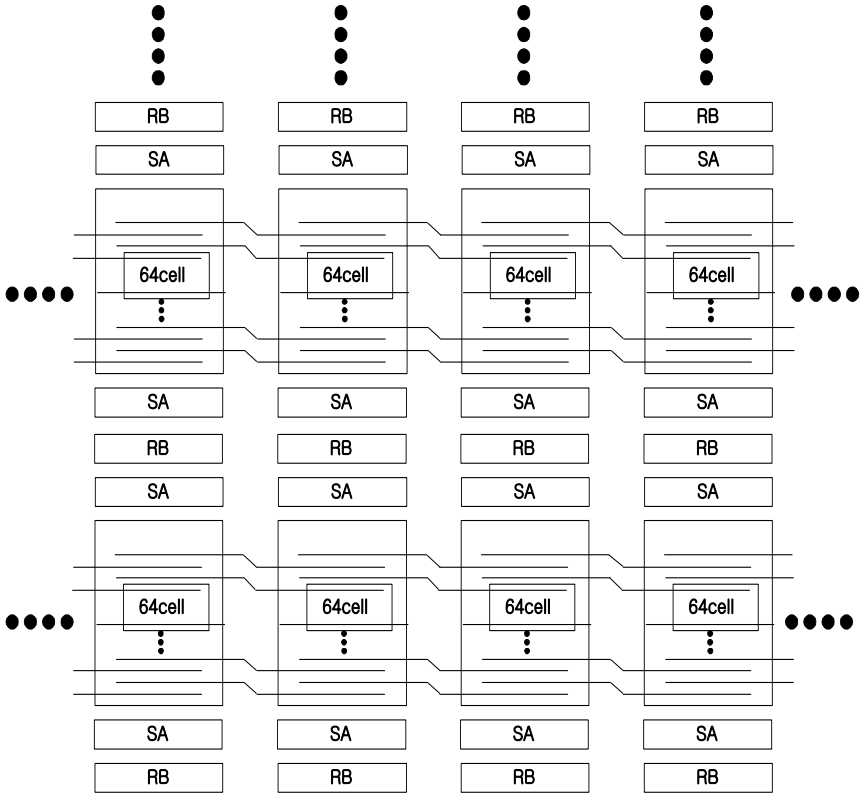
❑ Sub-Word Line 구조





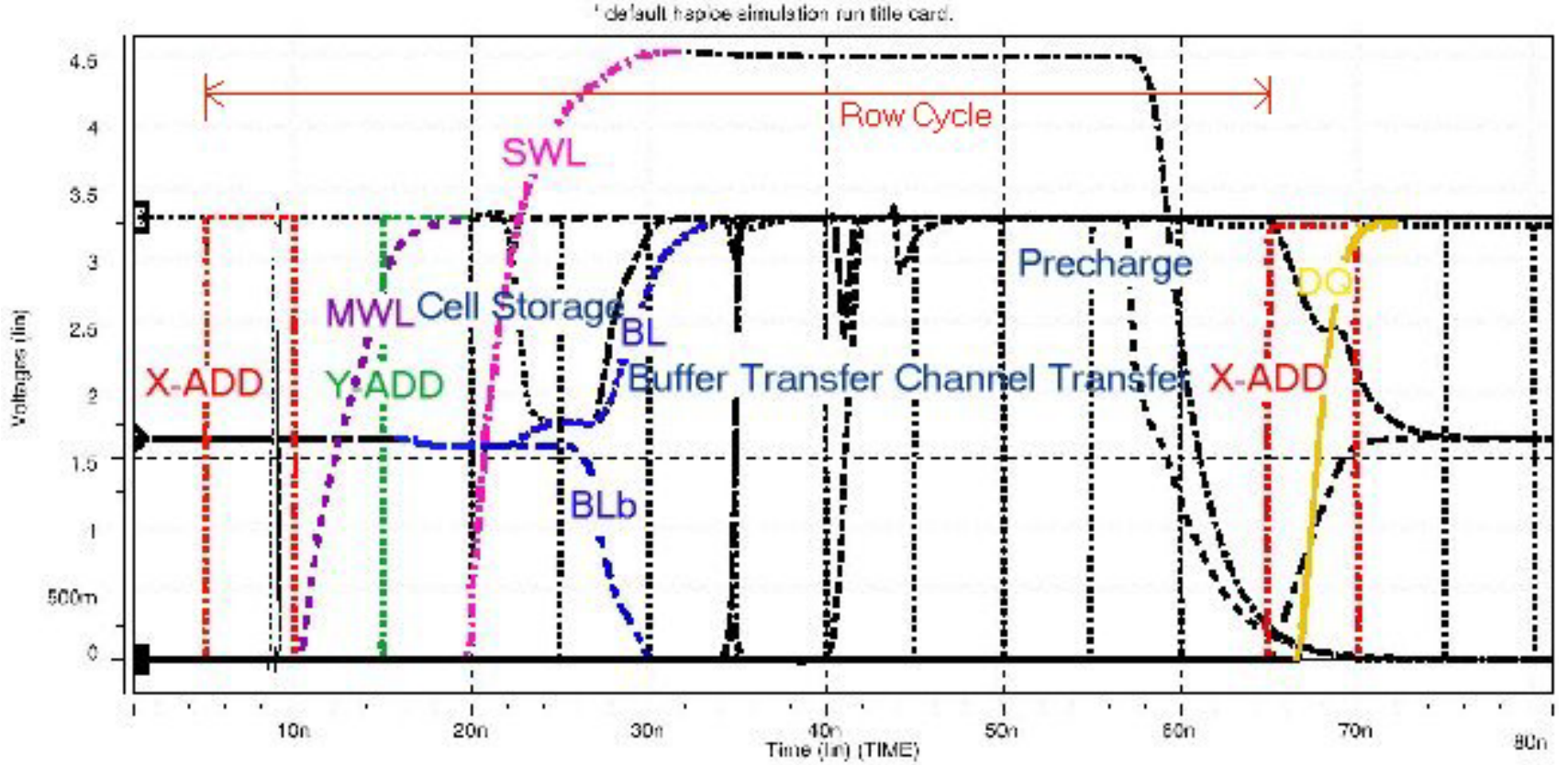
VPM Design (Gate Level)

- SPICE Simulation
  - 256 * 64 Sub-Block Array
    - Alternate Shared Sense Amp
    - 현대 0.35 μm
      - Word Line Model
        - » R : 23.4 KΩ
        - » C : 200 fF
      - Bit Line Model
        - » R : 8 KΩ
        - » C : 200 fF
  - 100MHz Clock



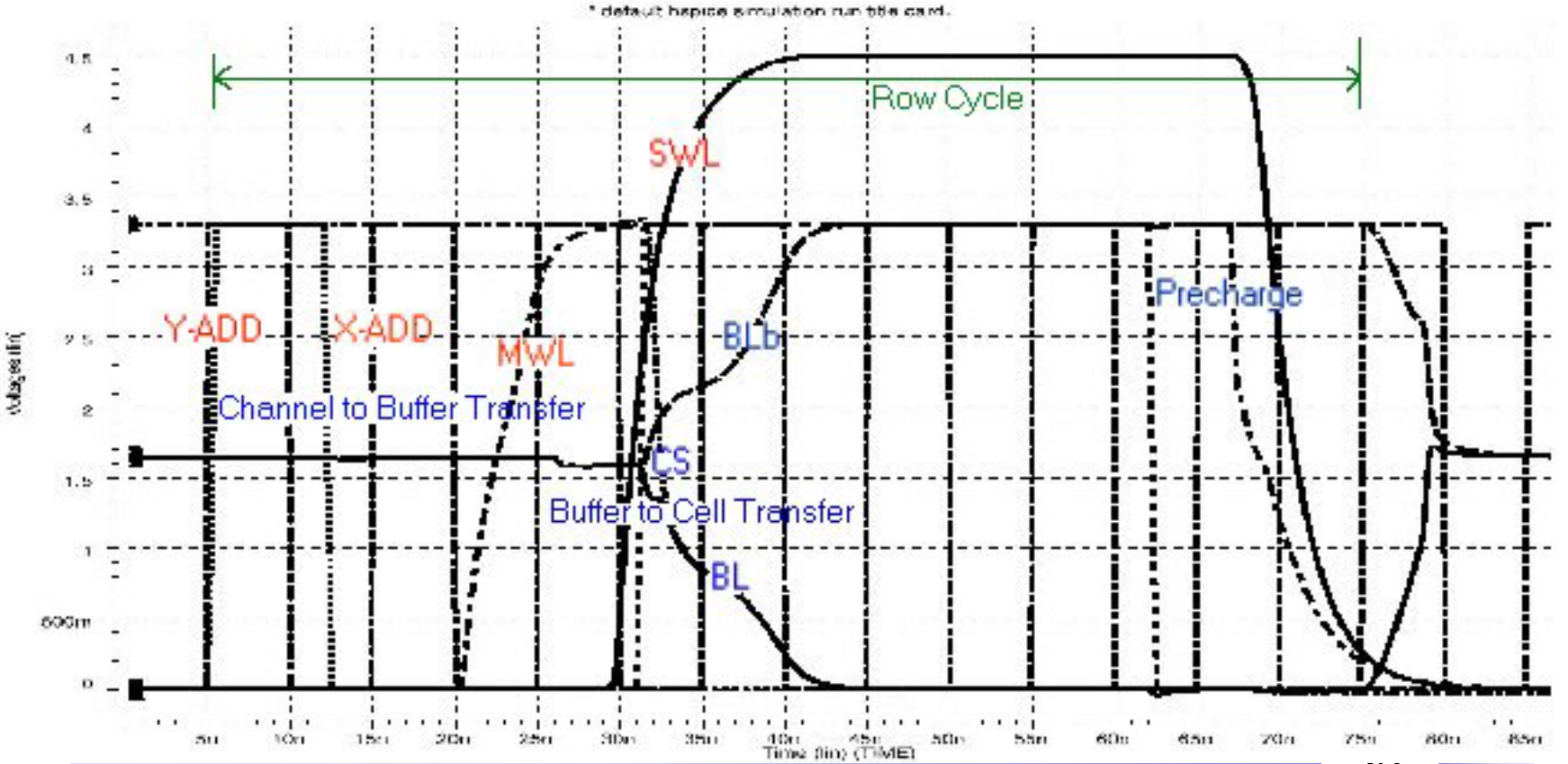
VPM Design (Gate Level)

❑ Cell Core to Channel Transfer (Prefetch)



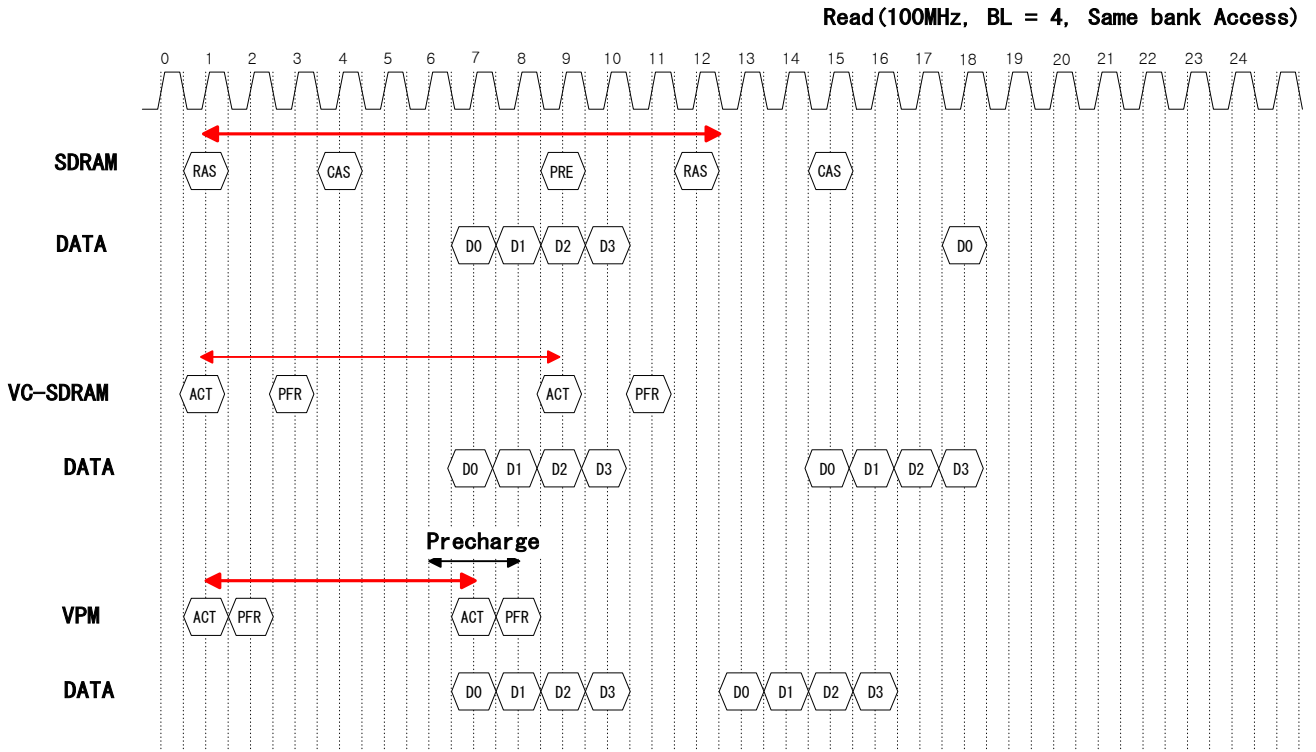
VPM Design (Gate Level)

❑ Channel to Cell Core (Restore)



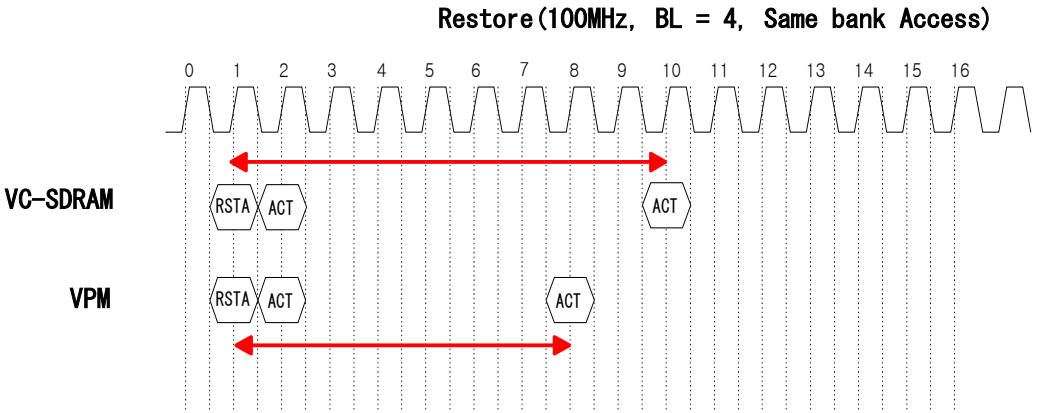
Row Cycle Comparison

❑ 연속적인 Read Access (100MHz, BL 4)

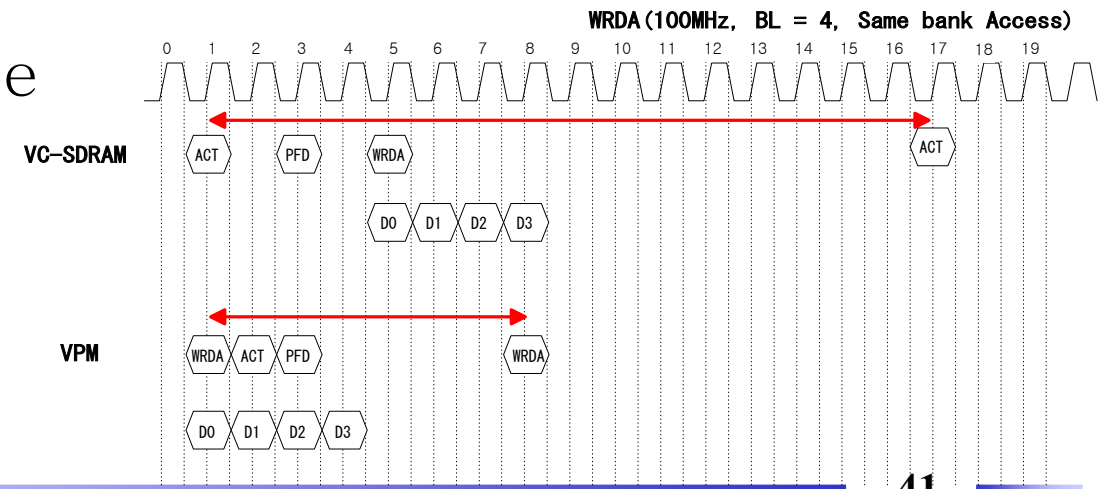


Row Cycle Comparison

❑ Restore Cycle

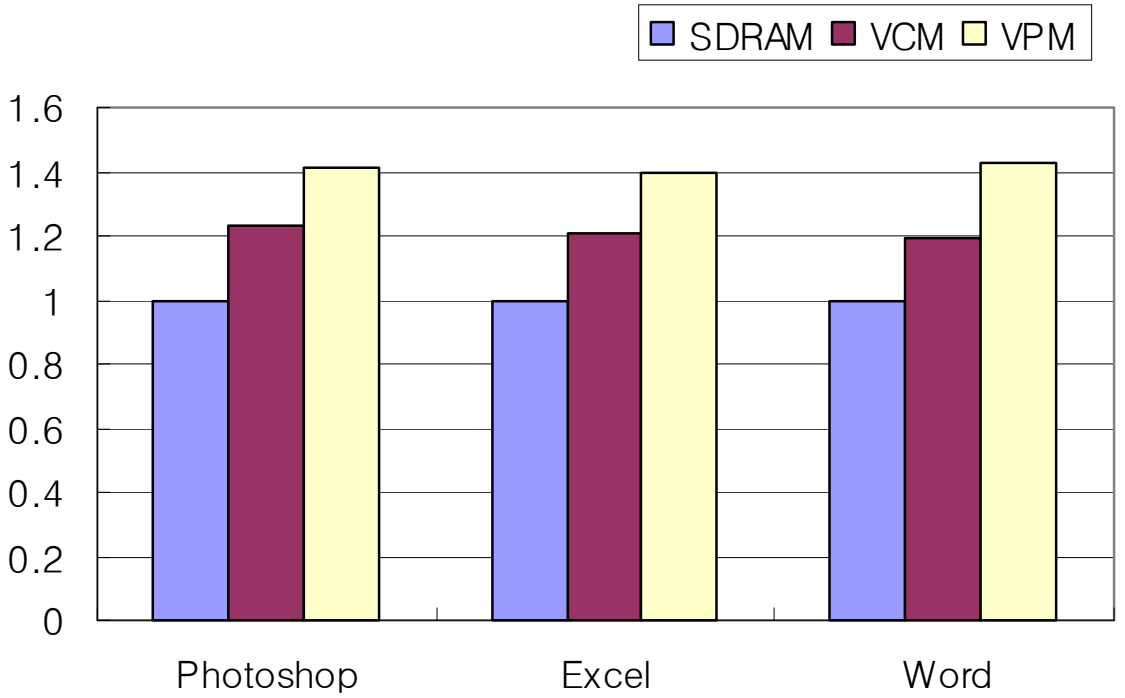


❑ Write Miss Cycle



성능 분석 : VPM

- Performance Analysis
  - Max. 40 %



결론 및 추후 과제

- 결론
  - Memory System 성능 분석기의 구현
    - VCM 구조의 성능 및 특성 분석
  - TOP Down 접근 방식을 사용한 VPM 구조 제안
    - VCM의 한계 극복
      - Fast Row Cycle
      - Low Power
- 추후 과제
  - VPM의 구현 (Layout)
  - VPM 구조의 EML 적용 가능성 검토